A Highly Integrated Multifunction Macro Synthesizer Chip (MMSC) for Applications in 2-18 GHz Synthesized Sources

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Abstract- Development and performance of a highly integrated multifunction MMIC for synthesizer applications are described. The chip forms the core of a synthesizer and does all the frequency selection and tuning. Measured performance up to 18 GHz is shown in this paper. With some modification to the architecture, it can support frequency generation through 40 Ghz. The chip has more than 30 RF functions integrated on an area of 4.27x4.68 mm². Some individual functions operate through 40 GHz.

I. Introduction

There is an urgent need to bring down the size and the manufacturing cost for high performance military and commercial systems. The MMIC technology can play a significant role by integrating as many functions as possible on a single chip without a big impact on yield and performance. Higher level of integration not only keeps the assembly cost down, it also increases the reliability by lowering the component count down. Recently commercial applications, at low radio frequencies (RF), have started utilizing MMICs that contain the whole transceiver (with possible exception of power amplifiers and oscillators) on a single chip [1], [2], [3]. The high level of multi function ($\geq$ 5) integration has been mainly accomplished at lower microwave frequencies ($\leq$ 10 GHz) using MESFET process. In this paper we will present the performance of a highly complex MMIC subsystem (>30 functions) that will form the core of a synthesized source. We have used 0.2μm PHEMT with high f_T process for the active devices. A careful trade-off study based on size of the chip, assembly cost and RF interconnects was made for this process to find the optimum number of functions that should be integrated on a single chip. For example, if more functions are integrated on a single chip, the integrated MMIC area drops when compared with the total area needed by individual MMICs. So the integrated MMIC cost drops until 25-35 functions above which the poor yield due to wafer variability cancels the effect of size advantage and the cost starts going up. Similarly, the assembly cost drops and reliability rises as more functions are integrated on the chip due to fewer RF interconnects (up to 25-35 functions on a single chip). The assembly cost starts to go up above 35 functions due to more complex supporting circuitry. With this trade-off in mind, we were able to integrate 33 rf blocks on a single chip.

We will henceforth refer to our chip as MMSC. The applications of MMSC are for both military electronic warfare systems and commercial portable test instruments (spectrum analyzers and network analyzers). The MMSC RF module is able to replace 60-70 percent of all RF functions in a typical commercial spectrum analyzer with nearly as much reduction in both volume and weight for the RF functions.

II. System Overview

The MMSC is designed to work in a synthesized source to produce an output frequency from 2 to 18 GHz. Fig. 1 shows the RF module incorporating the MMSC. The MMSC architecture itself is able to support any frequency range output provided the MMSC LO-chain is able to sustain the corresponding required frequencies in mm-wave range. The outputs at 672 MHz (Fig. 1) from the RF module are used to phase lock and fine tune the Narrow Band VCO (NBVCO) in conjunction with UHF synthesizer (500-1000 MHz). The overall system block diagram for the synthesizer demonstration unit is shown in Fig. 2. The RF MIC module needs some supporting functions such as a controller with control circuit assembly (CCA) and a UHF synthesizer. The CCA assembly provides the necessary control function to the RF module to tune the VCOs on MMSC. It also supplies a 1 GHz reference signal to the comb generator in MIC module to produce combs from 2 to 20 GHz and phase-locks the two 672 MHz signals coming from the MMSC and through the dividing chains in the RF module. The UHF synthesizer provides the UHF source (0.5-1 GHz) to fine tune a frequency between two discrete comb frequencies. The actual frequency selection and fine tuning scheme is explained in the document [4]. We will focus more on the MMSC part of it.

III. MMIC Design

The MMSC is designed using a commercially available PHEMT foundry process. It uses 0.2 μm devices with f_T up to 85 GHz. The MMSC chip photograph is shown in Fig. 3. Some of the critical chain responses are also shown in the figure. The LO chain has gain over 40 GHz. The simplified block diagram of the chip is shown in Fig. 4. The comb frequencies at 1 GHz apart are generated by the comb generator and input to the mixer M1 on MMSC. The mixer is double balanced with more than 25 dB isolation between comb-to-IF (21.5 GHz) and LO-to-IF. The LO to mixer is supplied by a set of Wide Band VCOs (WBVCO) that cover approximately 20 to 40 GHz. The exact lower and upper frequencies of the LO are determined by the IF and the coverage of the synthesized output. The WBVCOs are provided with a tune line and a quench line. The quench line is used to stop the VCOs totally when they are not being used. After the VCOs are combined through a three way combiner, the amplifiers in the LO

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chain boost up the LO to the appropriate levels of power to drive the mixers M1 and M2. The mixer M2 gives out the synthesized frequencies. M2 is a combination of two double-balanced mixers arranged in a spur-reject configuration to suppress the 2R/L products that give rise to inband crossover spurs. For example, with 30 GHz ≤ LO ≤ 31 Ghz and RF = 20.5 Ghz, the spurs 2R/L and output of the synthesized source will cross over between 10 and 10.5 GHz. The spur reject configuration suppresses the 2R products that are generated inside the diodes and then mixes with L to give 2R/L products. It does not suppress any 2R that may be associated with the signal R itself. The signal R for M2 is supplied by NBVCO, so 2R associated with NBVCO has to be filtered and NBVCO itself needs to be well shielded from M2. The spur reject mixer M2 improves the 2R/L suppression by 15-20 dBc. The double balanced version itself has approximately 50-60 dBc rejection of 2R/L (with RF = -20 dBm and LO = 12-13 dBm), so the combined effect is to sppress the inband spur more than 65 dBc down. This is more than adequate for any general pupose test instrument. The IF chain after the mixer M1 raises the power to 10 dBm for a dynamic divider to divide the IF frequency by 2. The LO amplifier chain is kept electrically isolated from the rest of the circuit to prevent any spurious signal amplification and consequently any unwanted spurs at the MMSC output. The LO chain also compensates for the power roll-off in the VCO at the high end of the band, so it has a positive gain slope from 23 to 41 GHz to keep the drive almost uniform over the LO frequency range.

IV. MEASURED PERFORMANCE

In this section we describe the measured data of a few critical blocks and the overall performance of the MMSC as it will operate in a synthesizer. One critical block of the MMSC is the LO amplifier chain. Fig. 5 shows the output power of one side of the LO that provides drive to the mixer M1. The response is shown at a nominal drive level of 5 dBm. The power output is adequate for M1. A similar measurement on the LO side providing power to M2 shows approximately 1.5 to 2 dB more power for the same drive level. The WBVCOs that act as the source have a slope on the power output that varies by ~15 dB over 20 to 40 GHz range, dropping from 0 dBm at 20 GHz to -15 dBm at 40 GHz. In order to compensate for this slope, the LO preamplifiers before the 90° Lange hybrid is designed to have a positive slope (Fig. 6). Fig. 6 shows the response of five single stages cascaded together. It has a slope of ~12-14 dB over 20 to 40 Ghz. Fig. 7 shows the output frequency spectrum of the MMSC at mixer M2. The mixer M2 is configured as two balanced mixers combined at the RF (NBVCO) side through a 90° hybrid and at IF side with an in-phase combiner. The in-phase combiner is built off-chip on alumina with a resistive network to save space. The combiner operates over 2 to 18 GHz. The LO is split in-phase to provide drive to the two balanced mixers in M2. The result is to cancel any 2R/L spurs that will be generated by the mixer itself. The frequency output is taken at two RF levels (-5 dBm and -10 dBm) to identify any 2R/L spurs and comb leakage from mixer input M1 to the output at M2. The comb leakage may be present and visible due to insufficient isolation between M1 input and the M2 output of the MMSC.

With the NBVCO fixed at 22.35 GHz and LO at 33.525 GHz, Fig. 7(a) shows output plots at 9, 11, 14 and 17 GHz (randomly chosen) of the MMSC at RF drive level of -5 dBm. Fig. 7(b) shows a similar plot at the same output frequencies at RF drive level of -10 dBm. Except for comb leakage from M1 to M2, the spur levels were found to be invisible over most of the output frequency band up to 16 GHz. At the frequencies ≥ 16 GHz, the 2R/L spurs become gradually visible. The reason for this is the weaker LO drive to the spur reject mixer M2 at LO frequencies ≥ 38 GHz ($f_{lo} = f_{rf} + f_{out} = 23.35 + 16 = 39.35$ GHz). A higher LO drive (>17 dBm) at ≥ 38 GHz is needed to avoid this problem. At -10 dBm RF power levels, the only visible spurs are the comb leakages. This problem can be minimized by carefully isolating the input to M1 from the MMSC output inside the MIC module. The spurs that need to be suppressed are the in-band cross-over ones. For example, with the RF (NBVCO) fixed at 22.35 Ghz, the cross-over spur occurs at L = 33.525 GHz and MMSC output at 11.175 GHz. Measurements between 11 and 12 GHz did not show any identifiable 2R/L spur except comb leakages.

V. CONCLUSION

We have shown a MMIC chip (MMSC) that contains more than 30 RF functions (some of them operating ≥ 40 GHz). The MMSC chip forms the core of the RF signal processing unit inside a frequency synthesizer. We have successfully shown the functionalities of the MMSC. The output frequencies above 16 GHz have visible 2R/L spurs because of weak LO drive above 38 GHz. To our knowledge, the MMSC is the first to have so many RF building blocks integrated on a single chip to perform a complex set of functions for a synthesizer. The next level of integration would be to accommodate the comb generator and the dividing chain on the same chip provided the yield on the process is high enough. The main challenge at a still higher level of integration will be to achieve the required level of isolation for various instrumentation. **This work was performed under the MIMIC PH-II contract (FY8558J22S) from DARPA.**

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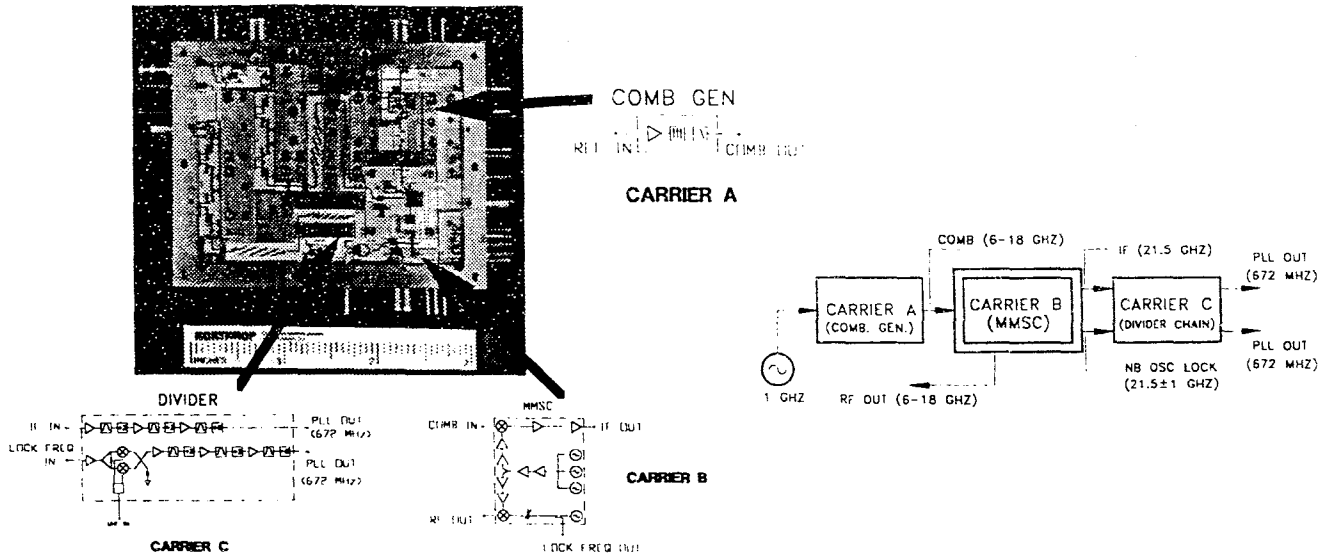

Figure 1 : RF MIC Module that incorporates the integrated MMSC. (a) The module assembly. (b) The block diagram of the MIC module showing the placement of MMSC.

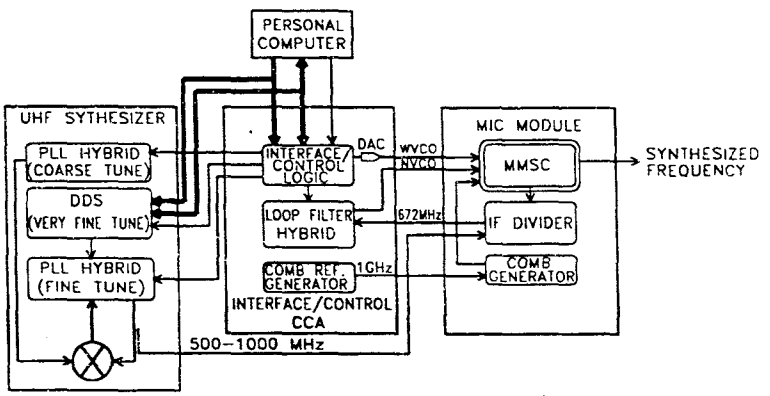

Figure 2 : System Overview block diagram for the MMSC demonstration. The MMSC is incorporated in the MIC (also called RF) module which in turn is supported by a control card assembly (CCA) and UHF synthesizer.

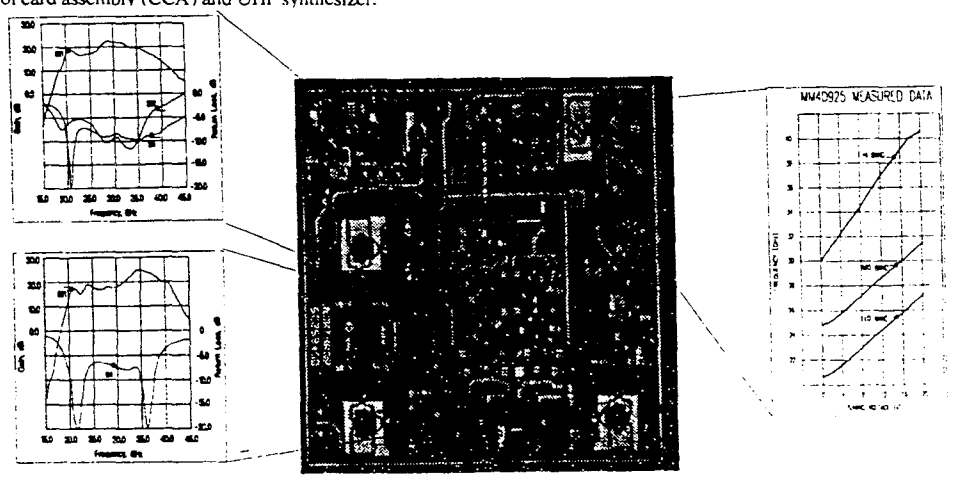

Figure 3 : MMSC photograph (4.27x4.68mm^2). It has more than 30 functions on a single chip, some operating up to 42 Ghz.

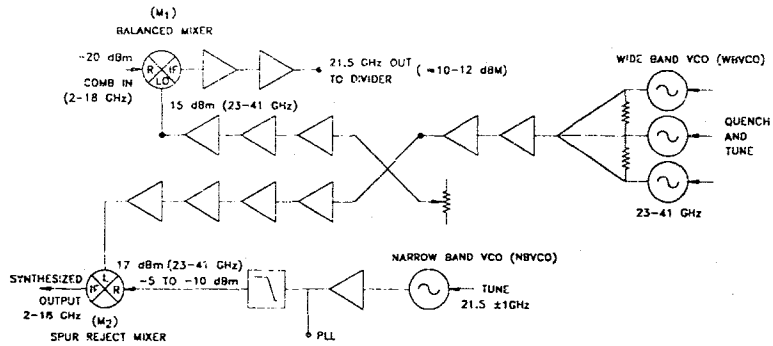

Figure 4 : Simplify block diagram for the MMSC. All the function blocks are not shown here.

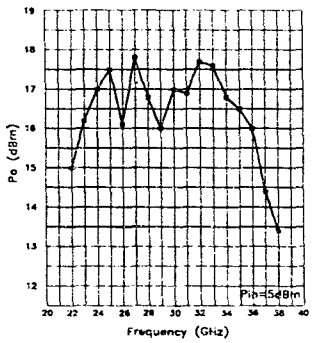

Figure 5 : Power output vs. Frequency of the LO amp to mixer M1 at Pin=5dBm.

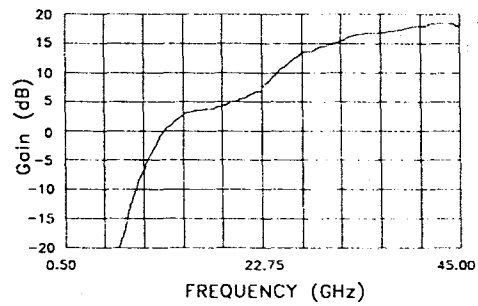

Figure 6 : Frequency response of the LO preamplifiers with a positive gain slope of 12-14 dB from 20-40 GHz.

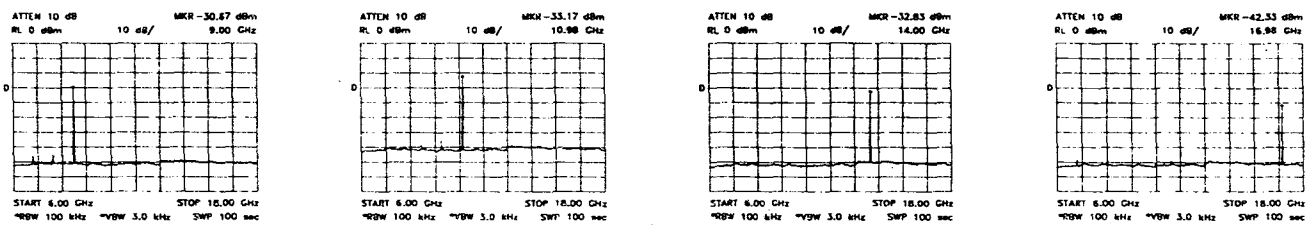

Figure 7(a)

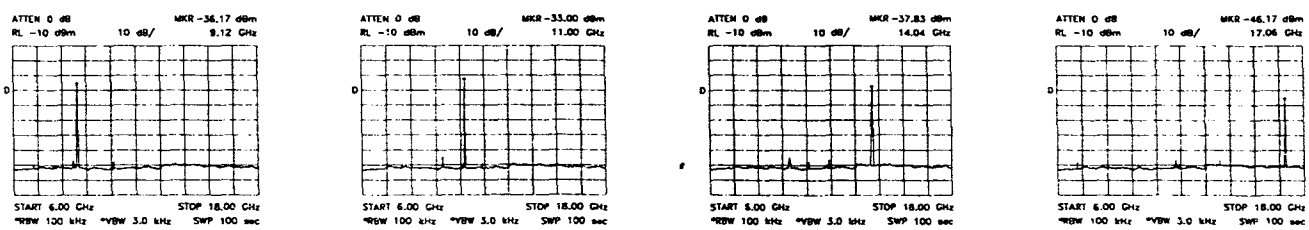

Figure 7(b)

Figure 7 : (a) Spectrum analyzer plots of MMSC output frequency (randomly chosen at 9, 11, 14, and 17 Ghz) with -10 dBm RF drive.
(b) Spectrum analyzer plots of MMSC output frequency (randomly chosen at 9, 11, 14, and 17 Ghz) with -5 dBm RF drive.